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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/778,029	02/17/2004	Hiroshi Ishiyama	118695	6188

25944 7590 11/15/2005

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EXAMINER	
PERALTA, GINETTE	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/778,029	ISHIYAMA, HIROSHI
	Examiner	Art Unit
	Ginette Peralta	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkouchi (U. S. Pat. 6,845,012 B2) in view of Fan (U. S. Pat. 6,773,964 B2) and Kodama et al. (U. S. Pat. 6,495,924 B2).

Regarding claim 1, Ohkouchi discloses in Fig. 1, a semiconductor module that comprises a semiconductor chip (101a, 101b) having a first surface and a second surface; a first electrode plate 103 contacting the first surface of the semiconductor chip (101a, 101b); a second electrode plate 102 contacting the second surface of the semiconductor chip (101a, 101b); and a resin mold 19 for sealing the first (103) and second (102) electrode plates and the semiconductor chip (101a, 101b).

Ohkouchi discloses the claimed invention with the exception of the resin mold including an inner pressure release portion.

Fan discloses in Figs. 3A and 3B, a semiconductor module that comprises a semiconductor chip having a first surface and a second surface; a first plate contacting the first surface of the semiconductor chip; a second plate contacting the second surface

of the semiconductor chip; and a mold (30 and 32) for sealing the first and second plates and the semiconductor chip; wherein the mold includes an inner pressure release portion 31 that passes from an interior of the mold to an exterior of the mold for releasing an inner pressure of the mold for the disclosed intended purpose of preventing a buildup of pressure throughout the lifespan of the IC package, as disclosed in col. 3, lines 42-52.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a mold that includes an inner pressure release portion that passes from an interior of the mold to an exterior of the mold as disclosed by Fan in the invention of Ohkouchi for the disclosed intended purpose of preventing a buildup of pressure throughout the lifespan of the IC package, as disclosed in col. 3, lines 42-52 of Fan.

Ohkouchi as modified by Fan discloses the claimed invention with the exception of the mold being a resin mold with the pressure release portion.

Kodama et al. discloses in Figs. 1, 2(a)-2(c), and 11, a semiconductor chip (1, 31) having a first surface and a second surface; a first electrode plate (3, 33) contacting the first surface of the semiconductor chip (1, 31); a second electrode plate (2, 32) contacting the second surface of the semiconductor chip (1, 31); and a resin (6, 42) that includes an inner pressure release portion for releasing an inner pressure in the module, wherein the resin that includes an inner pressure release for releasing an inner pressure in the module is taught for the disclosed intended purpose of accommodating the variation in

height of the contacting planes (warps, waviness, variation in dimensions of the members, and the like), and of decreasing the thermal resistance and electrical resistance at the contacting boundary plates as disclosed in col. 3, lines 4-9.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the semiconductor module of Ohkouchi a resin with an inner pressure release portion as Kodama teaches for the disclosed intended purpose of accommodating the variation in height of the contacting planes (warps, waviness, variation in dimensions of the members, and the like), and of decreasing the thermal resistance and electrical resistance at the contacting boundary plates as disclosed in col. 3, lines 4-9.

Regarding claim 2, Ohkouchi discloses that the first electrode plate 103 includes a first electrode and a signal terminal 103b, which protrude from the resin mold 19; and the second electrode plate 102 includes a second electrode 102, which protrudes from the resin mold, as shown in Fig. 1 and described in col. 5, lines 26-35.

Regarding claim 3, Ohkouchi as modified by Fan and Kodama et al. discloses that the inner pressure arises due to the temperature elevations resulting from the operation of the chip, as disclosed by Fan in col. 3, lines 42-52.

Regarding claim 4, Ohkouchi discloses in Fig.1 that the first electrode plate 103 includes a body, which is exposed outside of the resin mold 19; and wherein the second electrode plate 102 includes a body, which is exposed outside of the resin mold 19.

Regarding claim 5, Ohkouchi discloses in Fig. 1 that the semiconductor chip (101a, 101b) is sandwiched by the first and second electrode plates, 103 and 102, and embedded in the resin mold 19.

Regarding claim 6, Ohkouchi as modified by Kodama et al. discloses that the inner pressure release portion 6 is made of resin material having low adhesiveness to the resin mold, and wherein the inner pressure release portion 6 is a resin rod embedded in the resin mold as described in col. 6, lines 18-49, and col. 14, lines 36-67, and as shown in Figs. 2(a), 16, 17(a) and 17(b), where it is described that the portion 6 may comprise resin fibers coated with metal, and in Fig. 16 is shown an arrangement of the fibers surrounded by metal.

Regarding claim 7, Ohkouchi as modified by Kodama et al. discloses that the resin rod extends from a surface of the semiconductor chip to outside of the resin mold.

Regarding claim 8, Ohkouchi as modified by Kodama et al. discloses that the resin mold 19 includes a hole (region 104 of Ohkouchi), wherein the resin rod is inserted into the hole of the resin mold 19, and wherein the resin rod is removable from the hole so that a clearance is formed between the resin rod and the hole.

Regarding claim 9, Ohkouchi as modified by Kodama et al. discloses that the inner pressure release portion 6 works in such a manner that the inner pressure in the resin mold is released through the clearance between the resin rod and the hole.

Regarding claim 10, Ohkouchi as modified by Kodama et al. discloses that upon exerting pressure the rods can be flattened as shown in Fig. 2(c), and thus some of the fibers (rods) may be pushed out of the hole.

Regarding claim 11, Ohkouchi as modified by Kodama et al. discloses that the inner release portion 6 works in such a manner that the inner pressure in the resin mold is released through the hole after the resin rods or fibers drop out of the hole.

Regarding claim 12, Ohkouchi discloses in Fig. 1, a semiconductor module that comprises a semiconductor chip (101a, 101b) having a first surface and a second surface; a first electrode plate 103 contacting the first surface of the semiconductor chip (101a, 101b); a second electrode plate 102 contacting the second surface of the semiconductor chip (101a, 101b); and a resin mold 19 for sealing the first (103) and second (102) electrode plates and the semiconductor chip (101a, 101b).

Ohkouchi discloses the claimed invention with the exception of each of the first and second electrode plates includes an inner pressure release portion for releasing an inner pressure in the resin mold.

Fan discloses in Figs. 3A and 3B, a semiconductor module that comprises a semiconductor chip having a first surface and a second surface; a first plate contacting the first surface of the semiconductor chip; a second plate contacting the second surface of the semiconductor chip; and a mold (30 and 32) for sealing the first and second plates and the semiconductor chip; wherein the mold includes an inner pressure release portion 31 that passes from an interior of the mold to an exterior of the mold for

releasing an inner pressure of the mold for the disclosed intended purpose of preventing a buildup of pressure throughout the lifespan of the IC package, as disclosed in col. 3, lines 42-52.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a mold that includes an inner pressure release portion that passes from an interior of the mold to an exterior of the mold as disclosed by Fan in the invention of Ohkouchi for the disclosed intended purpose of preventing a buildup of pressure throughout the lifespan of the IC package, as disclosed in col. 3, lines 42-52 of Fan.

Ohkouchi as modified by Fan discloses the claimed invention with the exception of the mold being a resin mold with the pressure release portion.

Kodama et al. discloses in Figs. 1, 2(a)-2(c), and 10, a semiconductor chip (1, 31) having a first surface and a second surface; a first electrode plate (3, 33) contacting the first surface of the semiconductor chip (1, 31); a second electrode plate (2, 32) contacting the second surface of the semiconductor chip (1, 31); and a resin (6, 34, and 35) that includes an inner pressure release portion for releasing an inner pressure in the module, wherein in some embodiments the inner pressure release portion is included in the first electrode and in others is included in the second electrode plate; and wherein the resin that includes an inner pressure release for releasing an inner pressure in the module is taught for the disclosed intended purpose of accommodating the variation in height of the contacting planes (warps, waviness, variation in dimensions of the members, and

the like), and of decreasing the thermal resistance and electrical resistance at the contacting boundary plates as disclosed in col. 3, lines 4-9.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the semiconductor module of Ohkouchi a resin with an inner pressure release portion as Kodama teaches for the disclosed intended purpose of accommodating the variation in height of the contacting planes (warps, waviness, variation in dimensions of the members, and the like), and of decreasing the thermal resistance and electrical resistance at the contacting boundary plates as disclosed in col. 3, lines 4-9.

Regarding claim 13, Ohkouchi discloses that the first electrode plate 103 includes a first electrode and a signal terminal 103b, which protrude from the resin mold 19; and the second electrode plate 102 includes a second electrode 102, which protrudes from the resin mold, as shown in Fig. 1 and described in col. 5, lines 26-35.

Regarding claim 14, Ohkouchi as modified by Kodama et al. discloses that the inner pressure arises due to abnormal conditions such as warps, waviness, and the appearance of thermal and electrical resistances.

Regarding claim 15, Ohkouchi discloses in Fig.1 that the first electrode plate 103 includes a body, which is exposed outside of the resin mold 19; and wherein the second electrode plate 102 includes a body, which is exposed outside of the resin mold 19.

Regarding claim 16, Ohkouchi discloses in Fig. 1 that the semiconductor chip (101a, 101b) is sandwiched by the first and second electrode plates, 103 and 102, and embedded in the resin mold 19.

Regarding claim 17, Ohkouchi as modified by Kodama et al. discloses that the inner pressure release portion 6 is a starting point for deforming the first and second electrode plates so that the inner pressure is released.

Regarding claim 18, Ohkouchi as modified by Kodama et al. discloses that the starting point does not overlap the semiconductor chip.

Regarding claim 19, Ohkouchi as modified by Kodama et al. discloses that each of the first and second electrode plates includes the starting point and an other portion; and wherein the other portion is deformable so that a clearance is formed between the other portion and the resin mold 19.

Regarding claim 20, Ohkouchi as modified by Kodama et al. discloses that the inner pressure release portion (6, 34, 35) works in such a manner that the inner pressure in the resin mold is released through the clearance.

Regarding claim 21, Ohkouchi as modified by Kodama et al. discloses that the inner pressure release portion (6, 34, 35) is a concavity or convexity for deforming the first and second electrode plates so that the inner pressure is released.

Response to Arguments

3. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814